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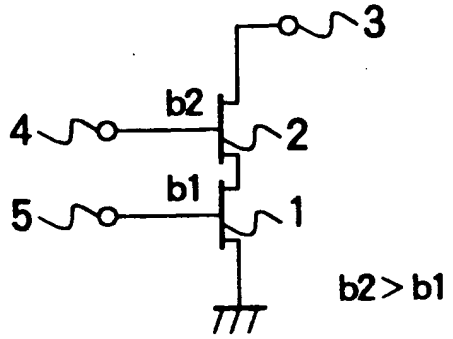
(54) Low-distortion cascode circuit.

(57) An electronic circuit is provided with a first field effect transistor (1) and a second field effect transistor (2), in which a drain of the first field effect transistor (1) connected to a source of the second field effect transistor (2). This electronic circuit inputs a first signal to a gate electrode (b1) of the first field effect transistor, inputs a second signal to a gate electrode (b2) of the second field effect transistor and outputs a signal from a drain (3) of the second field effect transistor. This electronic circuit is a cascode circuit related to the current drivability of the second field effect transistor is set to be larger than the current drivability of the first field effect transistor, and there is an effect that third-order or higher order distortion characteristics of a cascode type or dual-gate circuit can be reduced.

FIG. 1A



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BACKGROUND OF THE INVENTION

The present invention relates to a low-distortion cascode circuit for high-frequency communications, and relates more particularly to a low-distortion cascode circuit corresponding to a frequency converter or an amplifier of excellent low-distortion characteristics.

As a frequency converter (mixer) for a communication unit, a cascode circuit using a dual-gate field effect transistor (hereinafter to be referred to as a FET) has been widely known. An example of the conventional dual-gate FET is disclosed in the "GaAs Dual-Gate MESFETS's IEEE, Trans. Electron Devices, vol. ED-25, pp. 580-586", issued in June 1978.

The above-described prior-art technique is characterized in that the dimensions of two FET's are set the same. The prior-art dual-gate FET can be considered to be the cascode configuration of the FET's having almost the same electric characteristics.

The outline of a dual-gate FET which is operated as a frequency converter will be explained with reference to Fig. 6. Equivalent circuits of the dual-gate FET are shown as a cascode connection of two FET's 1 and 2. When the dual-gate FET is operated as a down-converter (mixer), an RF signal is applied to the gate of the lower-stage FET 1 from a terminal 5. A local signal is applied to the gate of the upper-stage FET 2 from a terminal 4. Functions of the FET's 1 and 2 will be explained below. The FET 1 functions as a voltage control type resistor which is modulated by an RF signal applied to the gate. The FET 2 has two functions. One is the function of a source follower for applying a local signal to the resistor. Since a local signal is applied to the resistor that has been modulated by the RF signal, a component of a product of both signals occurs in a current Id that flows through the resistor, so that a mixing function is achieved. The other function of the FET 2 is the function of an amplifier of a gate ground type. The current Id that flows through the resistor is outputted from the drain.

SUMMARY OF THE INVENTION

As described above, according to the prior-art technique, dimensions of the gates of the two FET's are set to be the same. There is also an example that the gate length of the second FET is set to be longer to have an improved breakdown voltage. This, however, has a problem that there is a risk of an occurrence of a distortion characteristics such as a third-order harmonic distortion, because the second FET can not operate as an ideal source follower or an ideal gate ground type amplifier as described above.

In order to identify the problems, an ideal operation will be compared with an actual operation, by taking an example that the first FET is being operated in a triode region. Assuming that a gate bias is expressed as Vg1, a drain bias is expressed as Vd1, a transconductance is expressed as b1 and a threshold voltage is expressed as Vth, then a drain current Id1 is given as follows:

$$Id1 = bl(Vgl - Vth)Vdl - 0.5Vdl^2 \quad \text{(Expression 1)}$$

where, "^2" represents a square. Assume that the FET 2 has operated as an ideal source follower and an ideal ground type amplifier. When a gate voltage and a drain current of the FET 2 are Vg2 and Id2, respectively, the following relations are obtained:

$$Id2 = Id1 \quad \text{(Expression 2)}$$

$$Vg2 - Vth = Vdl \quad \text{(Expression 3)}$$

from the expressions 1, 2 and 3, the following relation is obtained:

$$Id2 = bl(Vgl - Vth)(Vg2 - Vth) - 0.5(Vg2 - Vth)^2 \quad \text{(Expression 4)}$$

A term of bl*Vg1*Vg2 functions as a down converter. In the expression 4, there is no third-order or higher-order term relating to Vgl.

In comparison with the above, an actual operation of the FET 2 will be considered. Assuming that the FET 2 is being saturation operated, the following relation exists:

$$Id2 = b2(Vg2 - Vd1 - Vth)^2 \quad \text{(Expression 5)}$$

Based on the above expression, there is the following relation between Vd1 and the local Vg2:

$$Vd1 = Vg2 - Vth - SQRT(Id2/b2) \quad \text{(Expression 6)}$$

Based on the fact that the expression 2 is also established when the operation is not ideal and based on the expression 1, the following relation exists:

$$Id2 = b1(Vg1 - Vth)(Vg2 - Vth - SQRT(Id2/b2) - 0.5(Vg2 - Vth - SQRT(Id2/b2)^2 \quad \text{(Expression 7)}$$

While a detailed modification of the expression 7 will be omitted to avoid a complexity, because of the existence of the term "-SQRT(Id2/b2)" in the expression 7, a third-order or higher-order term relating to Vg1 will occur in the expression 7.

A frequency converter has been taken in the above as an example of the application of the cascode circuit. When the cascode circuit is applied as an amplifier in which the FET 1 saturation operates, a third-order term will also occur as shown below although the term is not so extreme as in the case of the frequency converter.

Id2 = bl(Vg1 - Vth)^2(1 + lambda*(Vg2 - Vth SQRT(Id2/b2)) (Expression 8)

According to the prior-art dual-gate FET, b1 = b2. In the second FET of which gate length has been made larger to improve the breakdown voltage, b1>b2. According to the above-described dual-gate FET, there has been a problem that there arises a significant influence of a third-order distortion as shown in the expression 7. It is an object of the present invention to provide a low-distortion cascode circuit in which the influence of the third-order distortion is minimized.

In order to achieve the above object, the low-distortion cascode circuit according to the present invention includes a first FET and a second FET, and the drain of the first FET is connected with the source of the second FET, a first signal is inputted to the gate electrode of the first FET, a second signal is inputted to the gate electrode of the second FET and a signal is taken out from the drain of the second FET, to form an electronic circuit, wherein the current drivability of the second FET is larger than the current drivability of the first FET. From a functional viewpoint, the above object can be achieved by setting the above-described b2 to be larger and bringing the operation of the FET 2 to closer to the operation of an ideal source follower and an ideal gate ground type amplifier.

When b2 is made to be larger, the current drivability of the FET 2 is increased straight. Methods for increasing the current drivability of the FET 2 by using many means will be explained in the following embodiments.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1C show a first embodiment of the present invention.

Figs. 2A and 2B show a second embodiment of the present invention.

Fig. 3 shows a third embodiment of the present invention.

Fig. 4 shows a fourth embodiment of the present invention.

Fig. 5 shows a fifth embodiment of the present invention.

Fig. 6 shows prior-art cascode circuit.

Figs. 7A and 7B show a sixth embodiment of the present invention.

Fig. 8 shows a seventh embodiment of the present invention.

Figs. 9A and 9B show an eighth embodiment of the present invention.

Fig. 10 shows a ninth embodiment of the present invention.

Fig. 11 shows a tenth embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of the present invention will be explained with reference to Figs. 1A to 1C. Of two cascode-connected FET's, a transconductance b2 of the upper-stage FET is set to be larger than a transconductance b1 of the lower-stage FET, to restrict a term of a third-order distortion or a higher-order distortion expressed by the expression 7. Setting b2 to be larger is nothing but increasing the current drivability of the FET 2.

As shown in Figs. 1A to 1C, the present invention provides an electronic circuit, including a first FET 1 and a second FET 2, according to which, a drain of the first FET 1 is connected with a source of the second FET 2, a first signal is inputted to a gate electrode of the first FET from a terminal 5, a second signal is inputted to the second FET from a terminal 4, and a signal is taken out from a drain of the second FET 2 to a terminal 3, wherein the current drivability of the second FET 2 is set to be larger than the current drivability of the first FET 1.

Methods for increasing the current drivability of the FET 2 by using many means in the embodiment will be explained below.

There are various methods for practically achieving b2>b1, such as, for example, setting a gate width W2 of the FET 2 to be larger than a gate width W1 of the FET 1 (reference Fig. 1B), setting a gate length L2 of the FET 2 to be shorter than a gate length L1 of the FET 1 (reference Fig. 1C), etc. D1 and D2 designate drains of the respective FET's, S1 and S2 designate sources of the respective FET's and G1 and G2 designate gates of the respective FET's.

A second embodiment of the present invention will be explained below with reference to Figs. 2A and 2B. The present embodiment shows the case that the cascode circuit is applied to the dual-gate FET and the lengths of the two gates G1 and G2 are differentiated to achieve b2>b1. The present embodiment is superior to the embodiment shown in Figs. 1A and 1C using the two FET's, in the chip area saving function when the circuit is integrated. Fig. 2A is a top plan view of the device and Fig. 2B is a cross-sectional view viewed from 1. P1 designates a substrate and OP1 designates a channel.

A third embodiment of the present invention will be explained with reference to Fig. 3. The present embodiment is an improvement of the current drivability and a reduction of a distortion by replacing the second FET 2 with a bipolar transistor 6. Other structures are the same as the structures of the embodiment shown in Figs. 1A and 1C.

A fourth embodiment of the present invention will be explained with reference to Fig. 4. According to the present embodiment, a local input from a terminal 8 is supplied to the second FET 2 through a source follower FET 7 so that a distortion which occurs when a signal source impedance is high is restricted. An emitter follower may be used in stead of the source follower. Other structures are the same as the structures of the embodiment of Figs. 1A to 1C.

A fifth embodiment of the present invention will be explained with reference to Fig. 5. The present embodiment aims at a reduction of an impedance at the source side of the second FET 2 by adding a feedback circuit 9 between the source and the gate of the second FET 2. Other structures are the same as the structures of the embodiment of Figs. 1A to 1C.

A sixth embodiment of the present invention will be explained with reference to Figs. 7A and 7B. The present embodiment achieves the cascode-connected FET of the embodiment shown in Figs. 1A to 1C by a dual-gate FET. The first FET 1 having a gate width W1 is cascode-connected with the second FET 2 having a gate width W2, to set W1 to be larger than W2. A channel structuring the drain of the FET 1 and a channel structuring the source of the FET 2 are set to be a common channel DS1 to achieve a cascode circuit in small area. Fig. 7A is a top plan view of the device of the present embodiment and Fig. 7B is a cross-sectional view of Fig. 7A viewed from a broken line 1. D2 and G2 designate a drain and a gate respectively of the second FET 2, S1 and G1 designate a source and a gate respectively of the first FET 1, OP1 and OP2 designate channels and P1 designate a substrate.

A seventh embodiment of the present invention will be explained with reference to Fig. 8. The present embodiment is an improvement to the dual-gate FET of the embodiment shown in Figs. 7A and 7B. In the embodiment shown in Figs. 7A and 7B, the channel structuring the drain of the first FET 1 and the channel structuring the source of the second FET 2 are connected by assuming the respective channel widths as W1 and W2. In this case, when the difference between W1 and W2 is extreme, there is a problem that there arises a significant difference between the current paths which flow through both ends of the FET's and the current path which flows through the center of the FET's. In order to mitigate this problem, according to the present embodiment, the shape of the common channel DS1 viewed from the top is set to be trapezoidal as shown in Fig. 8.

An eighth embodiment of the present invention will be explained with reference to Figs. 9A and 9B. According to the present embodiment, the common channel DS1 of the dual-gate FET of the embodiment shown in Figs. 7A and 7B is removed and the channel OP1 is set to be common. By removing the channel, the gate electrodes G1 and G2 can be set closer to each other so that the device is more compact than the device of the sixth embodiment.

A ninth embodiment of the present invention will be explained below with reference to Fig. 10. The present embodiment corresponds to a structuring of the first FET 1 in the embodiment of Fig. 8 by parallel connecting a plurality of transistors having a small gate width. The channel DS1 has a structure similar to the structure of the embodiment shown in Fig. 8. Fig. 10 shows an example of the structuring of the FET 1 by a parallel connection of three FET's. The gate width W1 of the first FET 1 is given by W1 = W11 + W12 + W13. By structuring the FET 1 in a parallel connection of a plurality of FET's as described above, a distortion of the current path when there is an extreme difference between W1 and W2 can be reduced. Although the present embodiment has been explained to have three FET's to structure the first FET 1, it is needless to mention that a similar effect can also be obtained when the number of FET's to be used to structure the FET 1 is changed.

A tenth embodiment of the present invention will be explained with reference to Fig. 11. The present embodiment corresponds to the embodiment of Fig. 10 where the structure of the channel DS1 is set similar to the structure of the embodiment shown in Fig. 9. The present embodiment relates to the feature that the gates G1 and G2 of the FET 1 and FET 2 exist on the same channel OP1.

In general, the channel has a larger resistance per unit area than the channel that structures source and drain electrodes, so that the former channel is easily affected by non-uniform current paths. Therefore, the parallel configuration of the FET 1 has a large effect of improvement.

Although description has been made above of the case where a cascode circuit is applied to a mixer circuit, it is needless to mention that all the above-described embodiments can also function as a low-distortion cascode amplifier by AC grounding the local input unit.

The present invention has an effect of reducing third-order or higher-order distortion characteristics of a cascode type or dual-gate type frequency

converter. The present invention can also function as a low-distortion cascode amplifier.

Claims

1. A low-distortion cascode circuit, comprising a first field effect transistor (1) and a second field effect transistor (2), with a drain (D1) of said first field effect transistor (1) being connected to a source (S2) of said second field effect transistor (2), including a first terminal (5) for inputting a first signal to a gate electrode (G1) of said first field effect transistor (1), a second terminal (4) for inputting a second signal to a gate electrode of said second field effect transistor and a third terminal (3) for outputting a signal from a drain of said second field effect transistor (2), wherein current drivability of said second field effect transistor (2) is set to be larger than current drivability of said first field effect transistor (1) (Figs. 1A ~ 1C).

2. A low-distortion cascode circuit according to Claim 1, wherein a gate width (W2) of said second field effect transistor (2) is set to be larger than a gate width (W1) of said first field effect transistor (1) (Fig. 1B).

3. A low-distortion cascode circuit according to Claim 1, wherein a gate length (L2) of said second field effect transistor (2) is set to be shorter than a gate length (L1) of said first field effect transistor (1) (Fig. 1C).

4. A low-distortion cascode circuit according to Claim 3, wherein said first and second field effect transistors (1 and 2) are structured by a dual-gate field effect transistor according to which said first gate (G1) and said second gate (G2) are formed on a same channel (OP1) to have different gate widths (Figs. 2A and 2B).

5. A low-distortion cascode circuit according to Claim 1, wherein said second field effect transistor (2) is displaced with a bipolar transistor (6), and a base is corresponded to a gate, an emitter is corresponded to a source and a drain is corresponded to a collector (Fig. 3).

6. A frequency converter in said low-distortion cascode circuit according to Claim 1, wherein a signal supply from said second terminal (4) to said second field effect transistor (2) is carried out through a source follower (7) (Fig. 4).

7. A frequency converter in said low-distortion cascode circuit according to Claim 1, wherein a feedback circuit (9) is provided for feedbacking from said source of said second field effect transistor (2) to said gate of said second field effect transistor (2) (Fig. 5).

8. A low-distortion cascode circuit according to Claim 2, wherein said first and second field effect transistors (1 and 2) are structured by a dual-gate field effect transistor according to which said drain of said first field effect transistor (1) and said source of said second field effect transistor (2) are shared by a common channel (DS1) (Figs. 7A and 7B).

9. A low-distortion cascode circuit according to Claim 8, wherein a plane shape of said channel (DS1) is changed to a trapezoidal shape (Fig. 8).

10. A low-distortion cascode circuit according to Claim 8, wherein said channel (DS1) is removed and a common channel (OP1) is provided common to said first and second field effect transistors (1 and 2) (Figs. 9A and 9B).

11. A low-distortion cascode circuit according to Claim 8, wherein said first field effect transistor is structured by parallel connecting a plurality of transistors (Fig. 10).

12. A frequency converter, comprising a first field effect transistor (1) and a second field effect transistor (2), with a drain of said first field effect transistor connected to a source of said second field effect transistor, to form an electronic circuit, for inputting a first signal to a gate electrode of said first field effect transistor, inputting a second signal to a gate electrode of said second field effect transistor and outputting a signal from a drain of said second field effect transistor, wherein a signal supply to said second field effect transistor is carried out through a source follower (7) (Fig. 4).

13. A frequency converter, comprising a first field effect transistor (1) and a second field effect transistor (2), with a drain of said first field effect transistor (1) connected to a source of said second field effect transistor (2), to form an electronic circuit, for inputting a first signal to a gate electrode of said first field effect transistor, inputting a second signal to a gate electrode of said second field effect transistor and outputting a signal from a drain of said second field effect transistor, wherein a feedback circuit (9) is provided for feedbacking from said source of said second field effect transistor (2) to said gate of said second field

effect transistor (2) (Fig. 5).

FIG. 1A

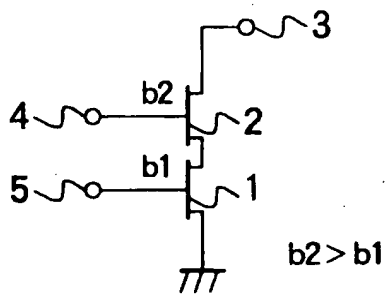

FIG. 1B

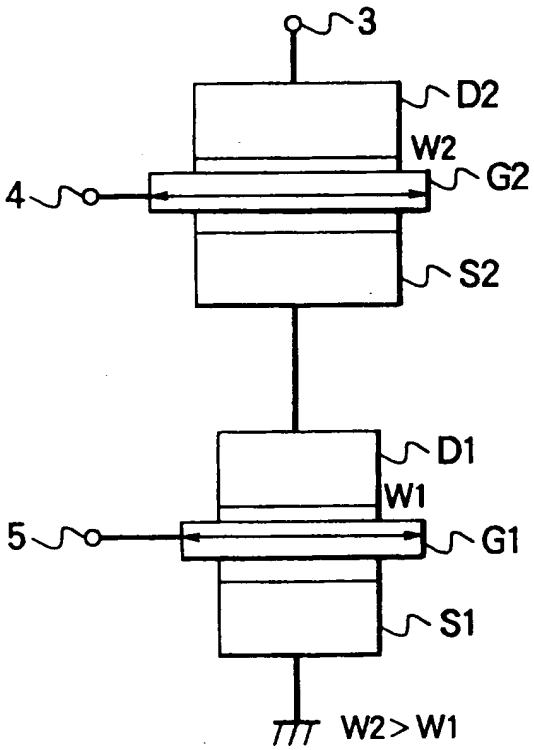

FIG. 1C

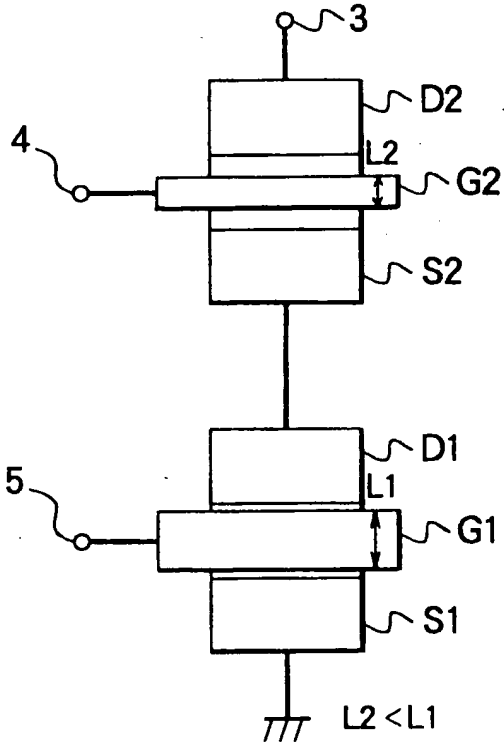

FIG. 2A

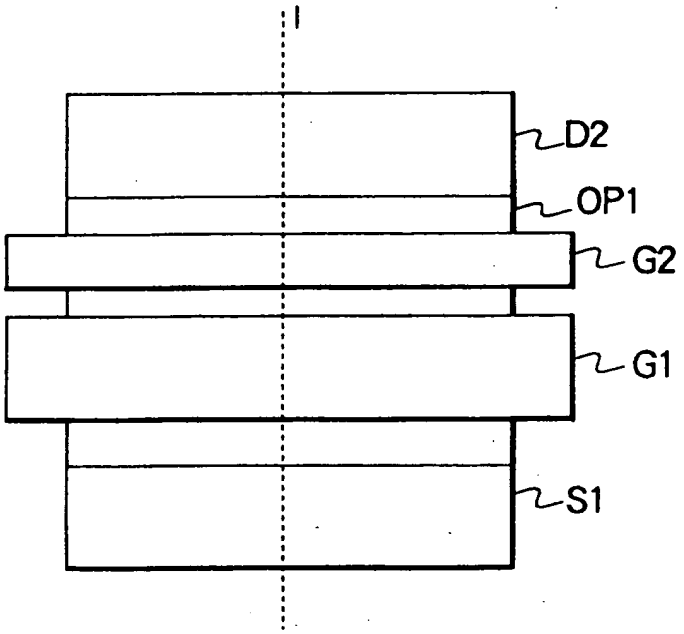

FIG. 2B

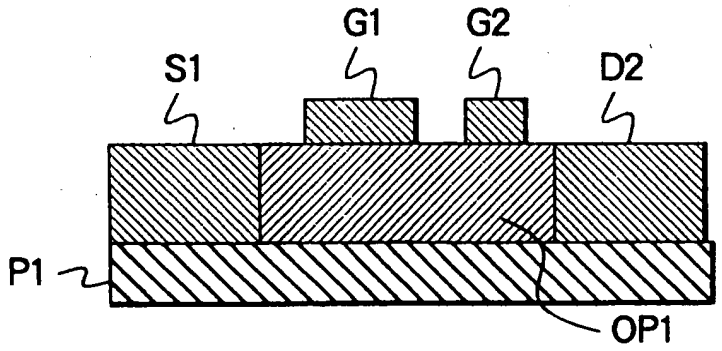

FIG. 3

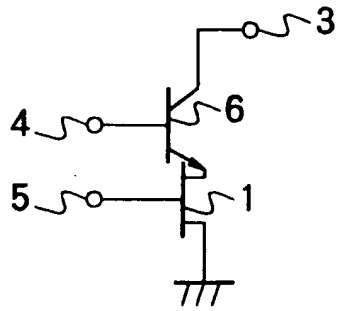

FIG. 4

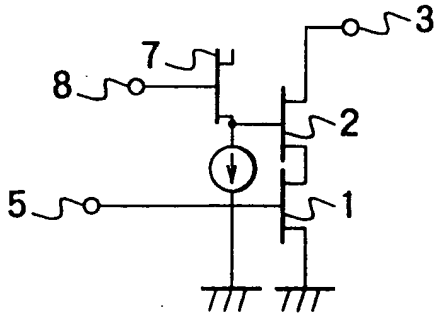

FIG. 5

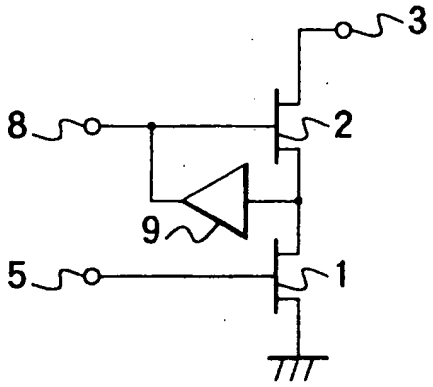

FIG. 6

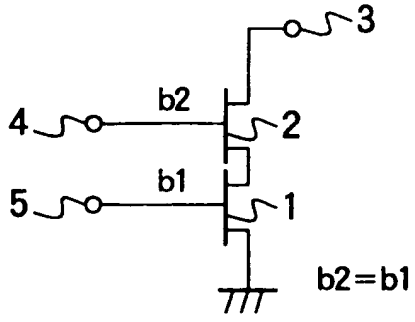

FIG. 7A

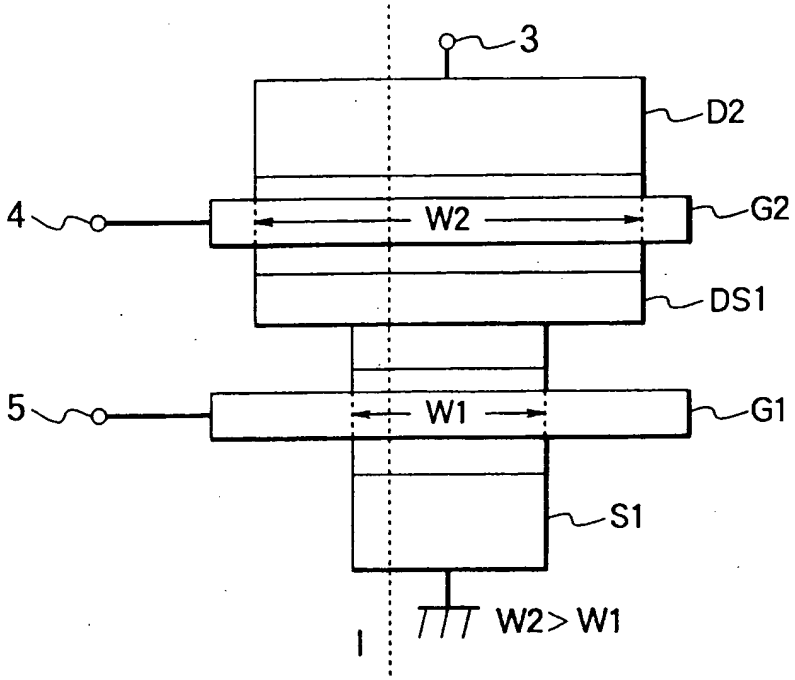

FIG. 7B

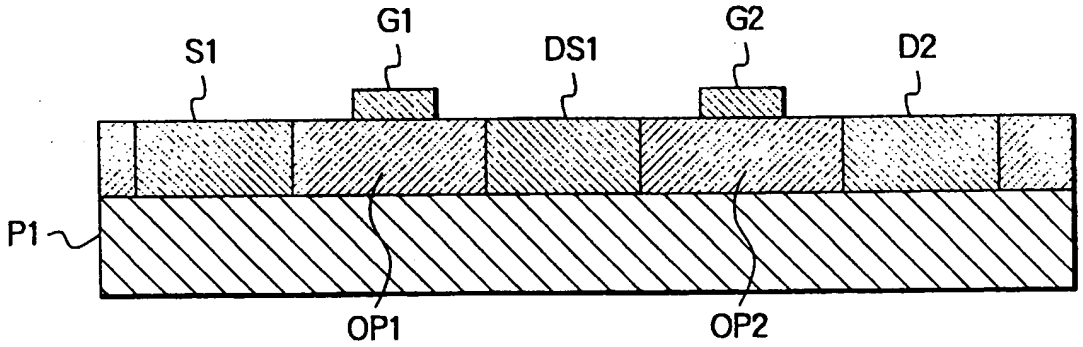

FIG. 8

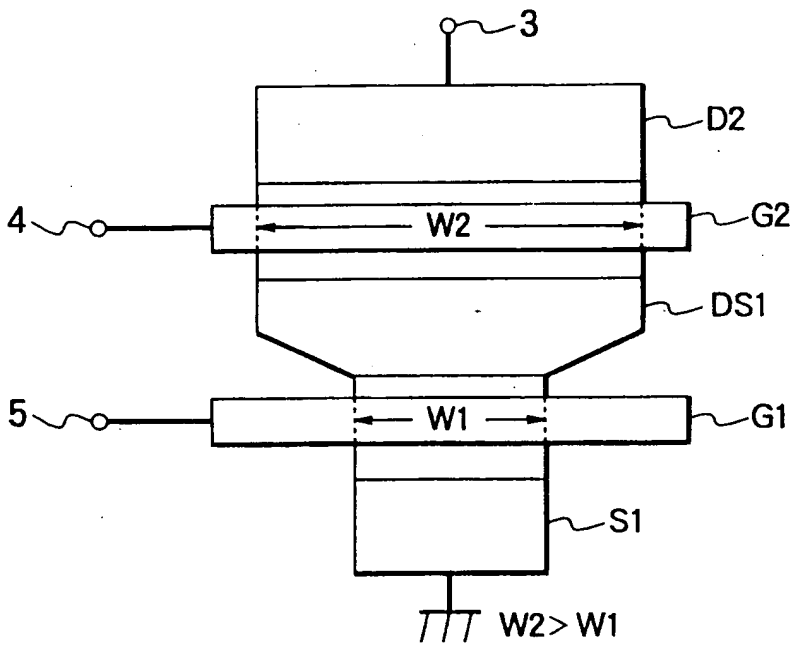

FIG. 9A

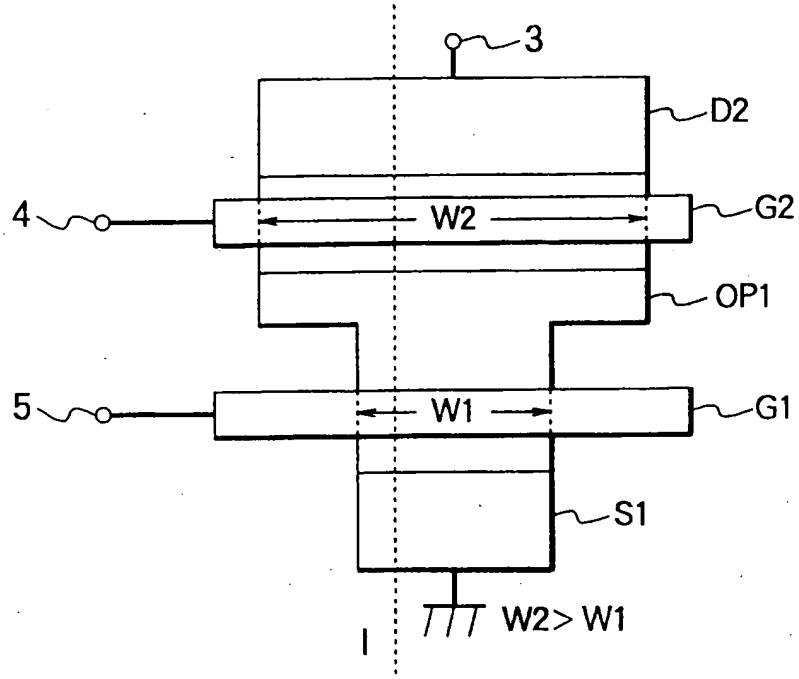

FIG. 9B

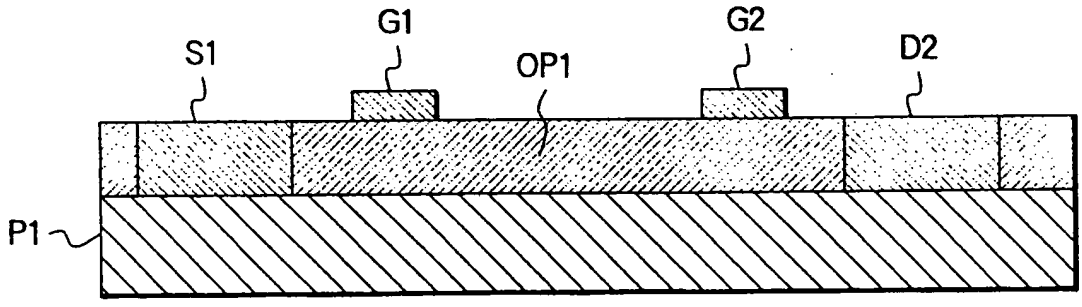

FIG. 10

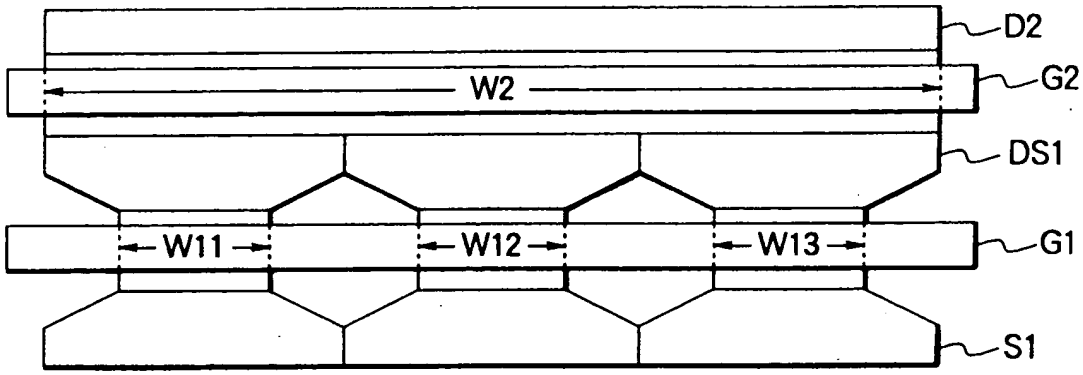
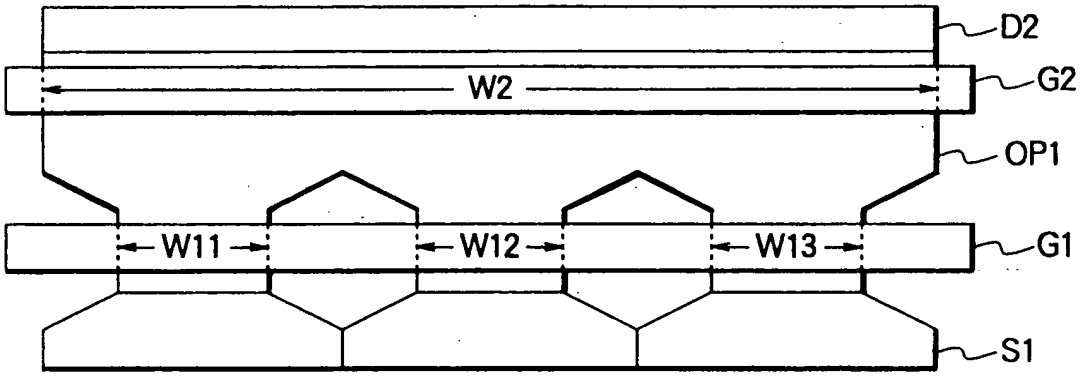
FIG. 11